REMARKS

This application has been carefully reviewed in light of the Office Action dated March 4, 2005. Applicants have amended claims 1, 3 - 5, 7, 9 -11. Reconsideration and favorable action in this case are respectfully requested.

The Examiner has requested a correction to paragraph [0032], which is provided herein. Further, paragraph [0011] was amended because it stated that the first signal (output of the VCO) and second signal (output of the divider) were compared to control the VCO. In fact, the output of the divider is compared with a reference signal as shown in the Figures and described in the text.

The Examiner has rejected claims 1-7 and 9-12 under 35 U.S.C. §102(b) as being unpatentable over U.S. Pat. No. 6,404,289 B1 to Su. Applicants have reviewed this reference in detail and do not believe that it discloses or makes obvious the invention as claimed.

The Examiner has rejected claim 8 under 35 U.S.C. §103 as being unpatentable over Su. Applicants do not believe that this reference discloses or makes obvious the invention as claimed.

Figures 6A-6C illustrate the method for finding a curve that includes the desired frequency and has the highest control voltage. Initially, in the search phase, the VCO 500 in Su is set such that the all capacitors 510 are enabled in the circuit, i.e., all switches 520 are closed (col. 6, line 52-61). The synthesizer attempts to reach lock (step 612). If lock cannot be achieved (step 614), the capacitor register is decremented to reduce the capacitance (step 616), which causes the VCO 500 to operate at the next level lower curve (col. 7, lines 6-8). The process of checking for lock at a particular value of the capacitor register, and decrementing the capacitor register if lock is cannot be obtained at that value, is repeated until lock is obtained (col. 7, lines 13-14). Once a lock condition is

found in step 614, the value of the control value used to obtain lock is checked (step 614). If the value is above or below upper or lower limits for the control voltage (step 630), a determination is made whether a lock condition can exist at another control voltage (step 632).

The method proposed by Su requires the frequency synthesizer attempt to lock at the desired frequency at every curve starting at the highest possible capacitive value. Accordingly, if lock can only be obtained at the lowest capacitive value, the search for a lock condition will result only after the synthesizer has attempted to lock at fifteen other capacitive combinations. A lock condition can only be evaluated on an active edge of the reference clock (fref in Su). At each active edge, a decision to increase or decrease the control voltage can be made (see Figure 3). Thus, it will take multiple fref clock cycles to determine whether lock can be obtained at given switched capacitor setting.

The present invention works in a completely different manner in order to accurately obtain the proper frequency range in the fastest time. First, a search for an initial control word to control the switched capacitors (and hence the frequency range of the VCO) is performed at a predetermined control voltage to the varactor (in the specification, the predetermined voltage is v_{cal}, set to the midpoint of the voltage range of the varactor). Using a predetermined control voltage on the varactor to perform the search will not be sufficient to definitively identify a single control word that will set the VCO to the desired frequency range. However, on each clock cycle of the reference frequency, it can be determined whether f_{cal} (the frequency provided at v_{cal} for the current control word setting) is greater than or less than f_{wanted}. However, it can narrow the search to an initial control word within an accuracy of +/- 1 to the correct control word. It should be noted that a less accurate search could also be used.

As an example, using the example of Su which has sixteen possible control words, this search can locate an initial control word in four reference clock cycles for a

dichotomizing search, or no more than sixteen clock cycles for a ramping search (such as the one shown in Su). It is unlikely that it would be possible to determine whether a locking condition exists for a *single* control word in Su within this time period.

Once the initial control word is found, it can be tested to see if the control word produces a frequency range in the VCO which contains f_{wanted}. In the specification, this is performed by checking the boundary conditions, i.e., v_{max} and v_{min}. If the condition $f_{max} \geq f_{wanted} \geq f_{min}$ (where f_{max} is the highest frequency produced by the VCO and f_{min} is the lowest frequency produced by the VCO within the boundary conditions), then the control word must be increased or decreased by one (assuming the search is accurate to +/-1). It should be noted that the determinations of $f_{wanted} \geq f_{min}$ and $f_{min} \geq f_{wanted}$, as shown in the flow chart of Figure 7, can each be made in one reference clock cycle. Accordingly, in the example above, using a dichotomizing search, the proper control word will be determined within *at most* six reference clock cycles (four for the initial search, and up to two clock cycles for the determination whether the control word should remain at the initial control word or should increase or decrease). It should be noted that the above analysis does not take into consideration of settling time between changing control words, which would effect both the present invention and Su.

If a search with an accuracy of greater than +/-1 was used, the detailed search would take longer, since the initial control word may be separated from the correct control word by more than one.

Accordingly, Applicants respectfully request allowance of claim 1 and dependent claims 2-6.

With regard to the Examiner's comment that there is no structure recitation in claims 2-6, Applicants strongly disagree. Each claim is directed towards the operation of the logic circuit. The operation of the logic circuit operates is a structural limitation.

The Examiner's comment that "the functional limitations can be performed by the prior art structure (Su et al)" is also traversed. Su operates in a specific fashion that is defined by the specification of Su. With regard to claim 3, Su does not test the initial control word by comparing the desired frequency to upper and lower bounds of a frequency range for the voltage controlled oscillator. As described above, Su checks the voltage at which locking occurred to upper and lower control limits for the voltage. This requires that the frequency synthesizer obtain lock before any checking can be done. As noted previously, this will require multiple clock cycles.

With regard to claim 4, Su does not determine an initial control word using fast comparisons between an actual frequency at the predetermined control voltage and the desired frequency. Su determines the appropriateness of a control word by determining whether a lock can be achieved. This requires comparisons at multiple frequencies through the entire control voltage range of the VCO.

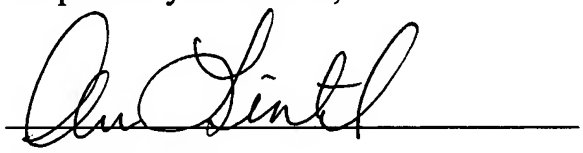
For reasons stated above in connection with claims 1 – 6, Applicants believe claims 7 – 12 are allowable as well.

The Commissioner is hereby authorized to charge any fees or credit any overpayment, including extension fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Alan W. Lintel, Applicants' Attorney at (972) 664-9595 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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Amendments to the Drawings:

The attached sheet of drawings includes changes to Figure 3. This sheet, which includes Figures 1 – 4, replaces the original sheet also including Figures 1 – 4. In Figure 3, reference numeral "10" has been replaced by reference numeral "20" for conformity with the specification.

Attachment: Replacement Sheet